SURAJKUMAR KADIYAM BALAJI

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EDUCATION

Northeastern University - Boston, MA **GPA : 4/4**
MS in Electrical and Computer Engineering (Microsystems Materials and Devices). **May 2026 (Expected)**
Coursework : Computer Architecture, Electronic Materials, VLSI Design, Solid State Devices

Anna University - Chennai, IN **GPA : 3.70/4**
BE in Electrical and Electronics Engineering (University Merit Scholar) **Sept 2018 – Jun 2022**
Coursework : Power Electronics, Embedded Systems, Digital Signal processing, Power System Operation and Control

SKILLS

Coding Languages : Python, C, C++, Embedded C, Verilog, System Verilog, UVM, Perl, TCL, Assembly Language
Software : Keysight ADS, Cadence (Virtuoso), STM32, TCAD, OrCAD, VESTA, PSPICE, Matlab, Xilinx ISE, Synopsys

WORK EXPERIENCE

Northeastern University – Boston, MA **Jan 2025 - Present**
Teaching Assistant – Fundamentals of Electronics
- Guided graduate students in Conducting Electronics experiments using lab equipment such as **Curve Tracer**, **Vector Network Analyser**
- Taught weekly **circuit** lab sessions, guiding students in simulation and enhancing presentation skills, while providing constructive feedback to 50+ students to improve performance.

Tata Technologies – Pune, IN **Jan 2023 – Jun 2024**
Electrical Design Engineer – Tata Motors Commercial Vehicles Team
- Tested and validated instrument clusters using **CAN** tools to meet performance and safety specs and reduced field failures by **20%** through simulation, diagnostic testing and **System Validation**.
- Performed signal integrity checks and **EMI/EMC** compliance testing using **STM32 IDE**, oscilloscope, and logic analyzers.
- Collaborated with cross-functional teams to troubleshoot analog front-end interfaces, reducing design cycle time.
- Collaborated with electrical and mechanical teams to resolve system integration issues and Cut fault diagnosis time by **30%** using **STM32 IDE**, **oscilloscope** and logic analyser tools.

Skill-Lync E-learning Company – Chennai, IN **Jul 2022 – Dec 2022**
Embedded Engineer Intern – Software Verification and Validation, AVR Bare Metal Team
- Developed real-time sensor interface on **STM32** using **FreeRTOS**, improving response latency by 40%.
- Implemented low-power modes and interrupts in **Embedded Firmware**, extending battery life by 55%.

PROJECTS

Design and Implementation of 32-bit ALU in 45nm using Cadence **Mar 2025**
- Designed a 32-bit ALU in 180nm CMOS using **Cadence Virtuoso** by scaling custom 1-bit ALU blocks.
- Applied Back Gate Forward Substrate Biasing to reduce delay by **~40%** and improve switching speed.
- Verified ALU performance via Spectre simulations using hierarchical schematics and testbenches.

Analysis of FinFET Technology for Analog and RF Applications **Mar 2025**
- Simulated 16nm FinFETs using **TCAD** and **Cadence** to analyse gain, leakage, and short-channel effects.
- Performed RF analysis using **Matlab** and **PSPICE** to extract S-parameters and frequency response.
- Performed **high-frequency S-parameter** analysis to validate performance for **RF** front-end blocks.
- Optimized fin dimensions to enhance fT and gm for low-power **analog front-end** blocks.

Functional Verification of HTAX Cross-bar using System Verilog & UVM **Mar 2025**
- Constructed **UVM** environment and applied formal verification of **RF/mixed-signal IPs** to ensure robustness aligned with hardware design standards
- Extracted logs with **Python Scripting** and conducted detailed coverage analysis in **IMC**, achieving **98%** coverage and integrated regression results in **VManager** to streamline tracking.
- Verified register functionality, access policies and coverage using **UVM** adapters , backdoor accesses.

Branch Prediction and Cache Design Simulator **Oct 2024**
- Evaluated adaptive Branch predictors using **Python**, improving accuracy by **26%** over 2-bit predictors on **SPECint2000**
- Built a Cache Simulator using **DineroIV**, achieving a **15%** boost in hit rates via Policy and Prefetch tuning
- Debugged Memory leaks, Segmentation faults and race conditions using **GDB** and **Valgrind** in **Linux** environments

CERTIFICATIONS

- Embedded C essentials - Skill-lync **Sep 2022**
- Software Verification and Validation - Skill-lync **Oct 2022**
- Verilog HDL : VLSI Hardware Design Masterclass - Udemy **May 2025**
- System Verilog for Design and Verification - Cadence **Aug 2025**

PUBLICATIONS

- Presented a paper at the IEEE-certified International Conference on Power, Energy, Control, and Transmission Systems and received a Certificate of Appreciation from the INSC Institute of Scholars **Dec 2022**
- Published research on Smart Wearable for Pulmonary Fibrosis patients in ICPECTS **Dec 2022**